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Per Hammarlund

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7590

08/22/2006

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EXAMINER

CERULLO, JEREMY S

ART UNIT

PAPER NUMBER

2112

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                                      |  |  |
|------------------------------|--------------------------------------|--|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/608,708 | <b>Applicant(s)</b><br>HAMMARLUND ET AL. |  |
|                              | <b>Examiner</b><br>Jeremy S. Cerullo | <b>Art Unit</b><br>2112                  |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7, 8, 13, 14, 16-19, 21-23 and 25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8, 13, 14, 17-19, 22, 23 and 25 is/are rejected.
- 7) ☐ Claim(s) 6, 17 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. Claims 1-5, 7, 8, 13, 14, 16-19, 21-23, and 25 are pending in the following action.

### ***Claim Rejections - 35 USC § 101***

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 22, 23, and 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 22, 23, and 25 are drawn to a machine-readable medium, which as described in the Specification in Paragraph [0072] on Page 24 may be signal transmissions. Signal transmissions are not considered tangibly embodied, and as such are not considered statutory subject matter.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-4, 13, 14, 18, 19, 22, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,493,741 ("Emer" et al.) in view of U.S. Patent No. 6,035,374 ("Panwar" et al.).

7. As for Claim 1, Emer teaches monitoring a node associated with a contended lock (address of a lock is equivalent to the node associated with a contended lock; Column 5, Line 28 – Column 6, Line 11), and putting an identified processor waiting for a lock (Column 5, Lines 51-61) to sleep until an event occurs at the lock address (placing a TPU into a quiesce mode is equivalent to putting it to sleep; Column 5, Line 62 – Column 6, Line 11). Emer does not teach the relinquishing of resources by the sleeping processor and including those resources in a larger set of resources to be used by non-sleeping processors. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be included in a larger set of

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resources available to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

8. As for Claims 2 and 3, Emer further teaches the use of pair of instructions (LDx\_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx\_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT.

9. As for Claim 4, Emer also teaches in Column 6, Lines 55-60, that the awakened processor acquires the resource after the resource is available.

10. As for Claims 13-14, in Column 5, Line 28 – Column 6, Line 11, Emer teaches a processor coupled with the storage medium (Figure 2, Item 100) with logic that allows the address of a lock (equivalent to the node associated with a contended lock) to be monitored, the monitoring comprising detection of the lock becoming available. Emer also teaches that an identified Thread Processing Unit (a logical processor) is put to sleep while waiting for lock until an event occurs at the lock address. Emer further discloses the use of pair of instructions in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). Emer does not teach the

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relinquishing of resources by the sleeping processor and including those resources in a larger set of resources to be used by non-sleeping processors. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be included in a larger set of resources available to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

11. As for Claims 18-19, in Column 5, Line 28 – Column 6, Line 11, Emer teaches a system with a storage medium (Figure 2, Item 137) and a processor coupled with the storage medium (Figure 2, Item 100) with logic that allows the address of a lock (equivalent to the node associated with a contended lock) to be monitored, the monitoring comprising detection of the lock becoming available. Emer also teaches that an identified Thread Processing Unit (a logical processor) is put to sleep while waiting for lock until an event occurs at the lock address. Emer further discloses the use of pair of instructions in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). Emer does not teach the relinquishing of resources by the sleeping processor and including those resources in a larger set of resources to be used by non-sleeping processors. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be included in a larger set of resources available to be used by other virtual processors (Column 8, Lines 33-44). It

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would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

12. As for Claims 22-23, in Column 5, Line 28 – Column 6, Line 11, Emer teaches a method in which the address of a lock (equivalent to the node associated with a contended lock) is monitored. Emer further teaches the use of pair of instructions (LDx\_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40; Column 6, Lines 55-60). It is inherent that in order for the computer to execute these instructions, they must be stored on a computer-readable medium. Emer does not teach the relinquishing of resources by the sleeping processor and including those resources in a larger set of resources to be used by non-sleeping processors. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be included in a larger set of resources available to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

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13. As for Claim 25, Emer also teaches in Column 6, Lines 55-60, that the awakened processor acquires the resource after the resource is available.

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14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Emer in view of U.S. Patent Application Publication No. 2003/0236816 (Venkatasubramanian, "Ven"). Emer and Panwar teach the limitations inherited from Claim 1 (See rejection above), but they do not teach that the processor is in a queue awaiting the release of the locked resource. However, in Paragraph [0003] on Page 1, Ven does teach the use of a sleep queue for threads waiting for a lock. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a queue as taught by Ven in the method of Emer in order to allow processors access to the resource in the order they requested it, preventing starvation of the sleeping processor.

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15. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer and Panwar as applied to Claims 1 and 13 above, and further in view of U.S. Patent Application Publication No. 2003/0126186 ("Rodgers" et al.).



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16. As for Claim 8, Emer and Panwar teach all of the limitations inherited from Claim 1. Panwar further teaches that when a processor sleeps and releases its resources, it releases the instruction queue by flushing its instructions (Column 8, Lines 33-44), but Panwar does not specifically teach what other resources are released. However, Rodgers teaches particular resources that are relinquished, including registers from a register pool, entries from a store buffer, and entries in a re-order buffer (Page 4, Paragraph [0047]). One of ordinary skill in the art at the time of the invention would have looked to available art to determine what additional resources utilized by a processor could be relinquished for the benefit of other processors. Finding Rodgers, it would have been obvious to have relinquished the registers, store buffer, and re-order buffer as taught by Rodgers, as well as the instruction queue as taught by Panwar.

17. As for Claim 17, Emer and Panwar teach all of the limitations inherited from Claim 13. Panwar further teaches that when a processor sleeps and releases its resources, it releases the instruction queue by flushing its instructions (Column 8, Lines 33-44), but Panwar does not specifically teach what other resources are released. However, Rodgers teaches particular resources that are relinquished, including registers from a register pool, entries from a store buffer, and entries in a re-order buffer (Page 4, Paragraph [0047]). One of ordinary skill in the art at the time of the invention would have looked to available art to determine what additional resources utilized by a processor could be relinquished for the benefit of other processors. Finding Rodgers, it

would have been obvious to have relinquished the registers, store buffer, and re-order buffer as taught by Rodgers, as well as the instruction queue as taught by Panwar.

### ***Allowable Subject Matter***

18. Claims 7, 16, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19.

20. The following is a statement of reasons for the indication of allowable subject matter:

21. Claim 7 contains allowable subject matter, particularly the limitation that the waking up of the processor comprises reacquiring the same resources that it had relinquished when put to sleep.

22. Claim 16 contains allowable subject matter, particularly the limitation that the waking up of the processor comprises reacquiring the same resources that it had relinquished when put to sleep.

23. Claim 21 contains allowable subject matter, particularly the limitation that the waking up of the processor comprises reacquiring the same resources that it had relinquished when put to sleep.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 8:00-4:00; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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8/19/06